PRO-LOG
CORPORATION

STD 7000

7501
Medium Power
DC Driver Card

USER'S MANUAL

7501
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USER'S MANUAL

PRELIMINARY

PRO-LOG
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FORWARD

This manual explains how to use Pro-Log's 7501 Medium Power DC Driver Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7501. We welcome your suggestions on how we can improve our instructions.

The 7501 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use microprocessors and the STD BUS products.

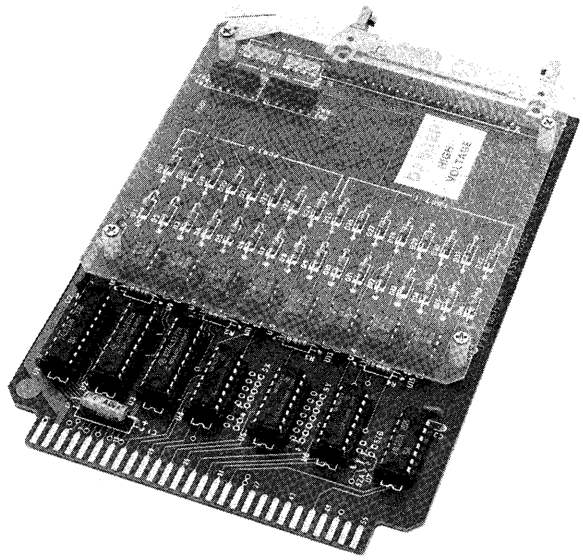
You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual*. If you would like a copy of these documents, please submit your request on your company letterhead.

7501 MEDIUM POWER DC DRIVER CARD

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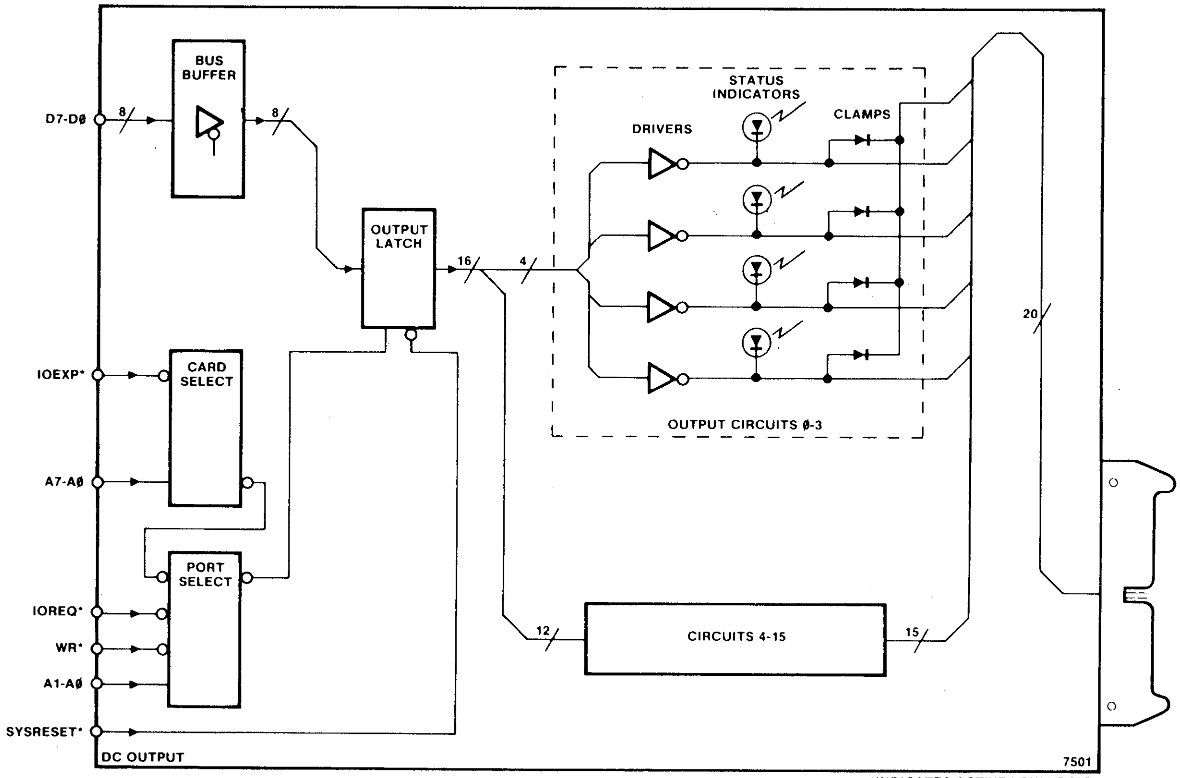
7000 STD BUS MEDIUM POWER DC DRIVER CARD 7501

The 7501 provides sixteen independent DC output circuits for the 7000 Series STD BUS. Each open collector output circuit is capable of sinking up to +225mA of current in the on-state and can withstand a +50V output level in the off-state. Diode clamping is included to limit the output voltage when driving inductive loads. Separate user-supplied clamp voltage inputs are provided for each group of four outputs. Sixteen LEDs provide a visual indication of the state of each output.



FEATURES

- 16 Independent DC Output Circuits
- +225mA Current Sink Rate
- +50V Output Rating
- Diode Clamp for Driving Inductive Loads
- Ground Return for each Output Circuit
- LED Indicator for each Output Circuit
- Standard 40-pin Flat Cable Connector
- Clear Plastic Safety Shields



*INDICATES ACTIVE LOW LOGIC

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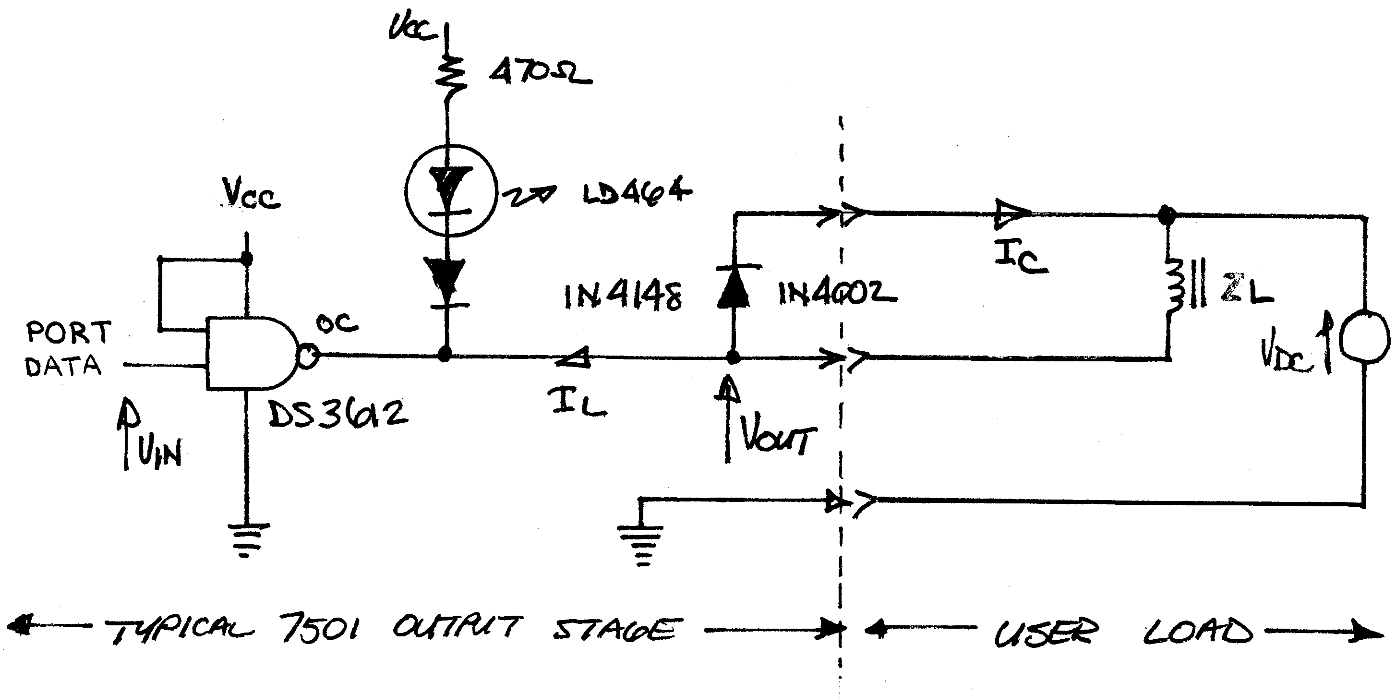
SECTION 2

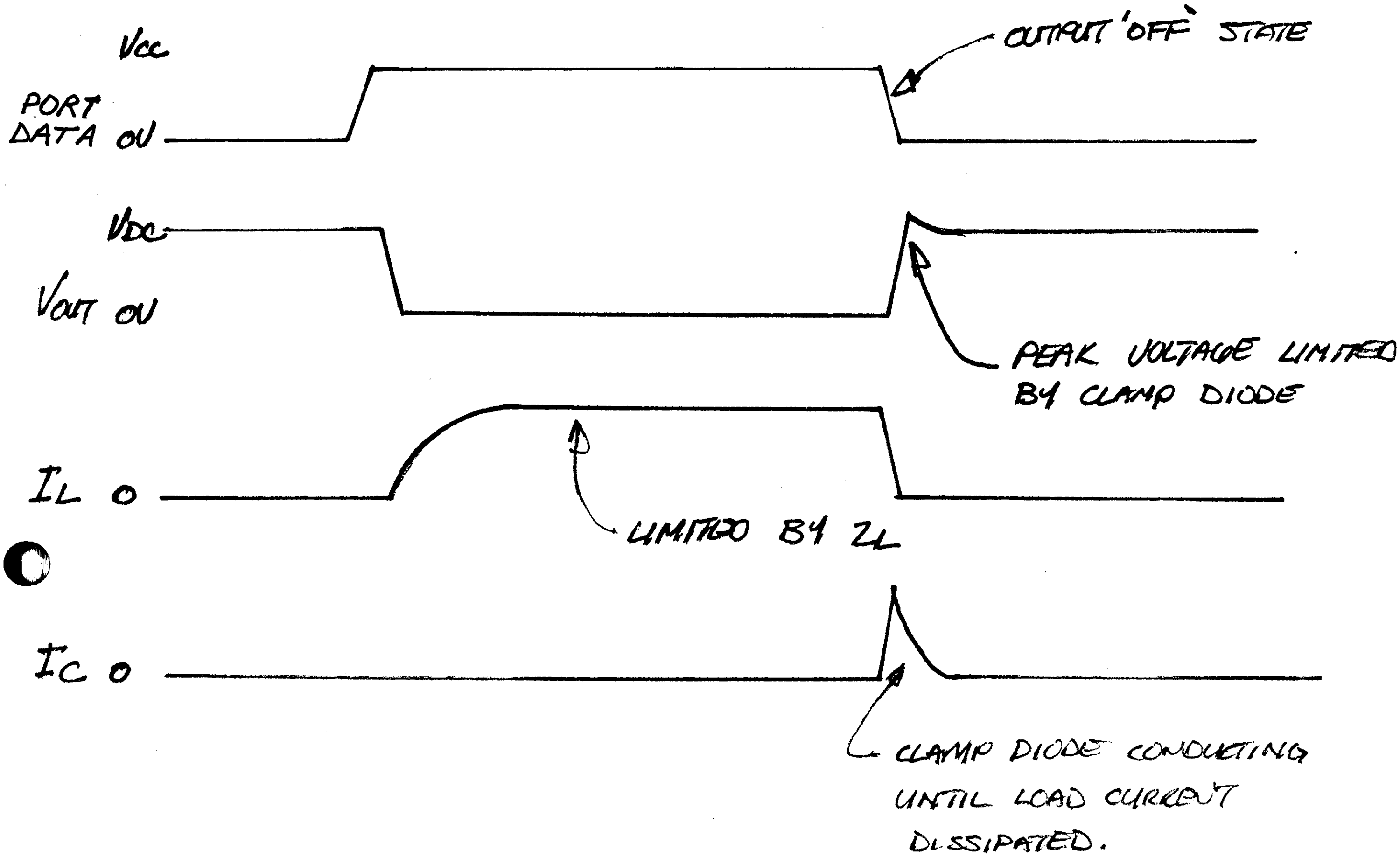
FUNCTIONAL

Operation

The 7501 converts TTL level signals supplied by the STD BUS to latched, negative true, open-collector DC drive signals. This conversion process begins by strobing eight bits of data into one of two fully decoded write-only output port latches. These latches are cleared at power on by the SYSRESET* signal. A medium power logic driver, as shown in the accompanying figures, converts the sixteen latched output signals to an inverted, open collector signal. The driver's outputs are then brought to a 40-pin flat cable connector at the user interface card edge. Alternating ground and output wires minimize crosstalk on the flat cable.

When driving inductive loads, a diode clamp protects each medium power logic driver output from high voltage breakdown. This diode is connected between the user-supplied clamp voltage (+50V or less) and the output signal line. When the logic driver is switched off (no current sink), the inductive current surge raises the collector output voltage above normal levels. When the output voltage exceeds the clamp voltage, the clamp diode will limit the collector voltage to approximately the clamp voltage. A separate clamp voltage input is provided for each group of four outputs (16 outputs, 4 groups) at the user interface connector. The clamp voltage must be greater than or equal to the off-state output voltage for each output, but less than +50V. All output signals are monitored for the low (active) state by LEDs. A diode protects each LED from reverse voltage breakdown.





Vcc
PORT DATA 0V
OUTPUT 'OFF' STATE
VDC
VOUT 0V
PEAK VOLTAGE LIMITED BY CLAMP DIODE
IL 0
LIMITED BY ZL
IC 0
CLAMP DIODE CONDUCTING UNTIL LOAD CURRENT DISSIPATED.

SECTION 3

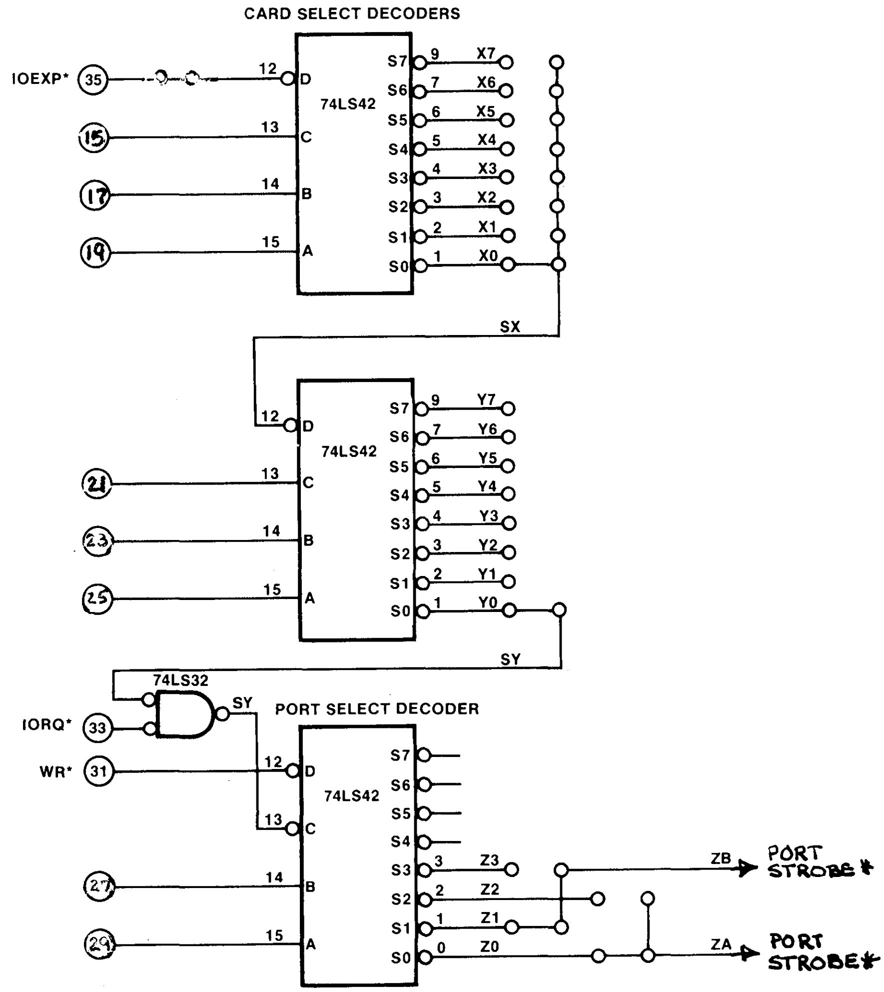
MAPPING

The 7501 consists of two 8-bit output ports that may be placed anywhere in the I/O address space of 00-FF. These ports occupy two consecutive address locations. The 7501 is shipped with hexadecimal port address 40 (port 0 address) and port address 41 (port 1 address). These port addresses are selected by jumper wires. To remap the 7501 to another address set, the user connects one jumper wire on each of SX, SY, SZA and SZB as shown in the Card Address Selection diagram.

The I/O address mapping and jumper selection table for 2 addresses per card shows where to place jumper straps to obtain any two sequential port addresses in the hexadecimal range 00-FF. Using the lowest of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along this vertical axis, and the least significant hex digit on the horizontal axis. For example, port addresses 40 and 41 are obtained by connecting jumpers at X2, Y0, Z0 and Z1.

The only restriction that applies in address selection for the 7501 is the lower of the two port addresses (40 as shipped) must occur only at every second possible address. For example, the sequence 41 and 42 is not allowed by the decoder.

The pad matrices adjacent to U4, U5 and U6 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.



I/O Address Decoder And Schematic For 2 Addresses Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X, Y & Z
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	← z
0		X0	Y0			X0	Y1			X0	Y2			X0	Y3		
1		X0	Y4			X0	Y5			X0	Y6			X0	Y7		
2		X1	Y0			X1	Y1			X1	Y2			X1	Y3		
3		X1	Y4			X1	Y5			X1	Y6			X1	Y7		
4		X2	Y0			X2	Y1			X2	Y2			X2	Y3		
5		X2	Y4			X2	Y5			X2	Y6			X2	Y7		
6		X3	Y0			X3	Y1			X3	Y2			X3	Y3		X
7		X3	Y4			X3	Y5			X3	Y6			X3	Y7		
8		X4	Y0			X4	Y1			X4	Y2			X4	Y3		AND
9		X4	Y4			X4	Y5			X4	Y6			X4	Y7		Y
A		X5	Y0			X5	Y1			X5	Y2			X5	Y3		
B		X5	Y4			X5	Y5			X5	Y6			X5	Y7		
C		X6	Y0			X6	Y1			X6	Y2			X6	Y3		
D		X6	Y4			X6	Y5			X6	Y6			X6	Y7		
E		X7	Y0			X7	Y1			X7	Y2			X7	Y3		
F		X7	Y4			X7	Y5			X7	Y6			X7	Y7		

I/O Address Mapping and Jumper Selection Table for 2 Addresses Per Card.

ADDRESS DECODER OPERATION

Refer to the shcematic, Document #105194

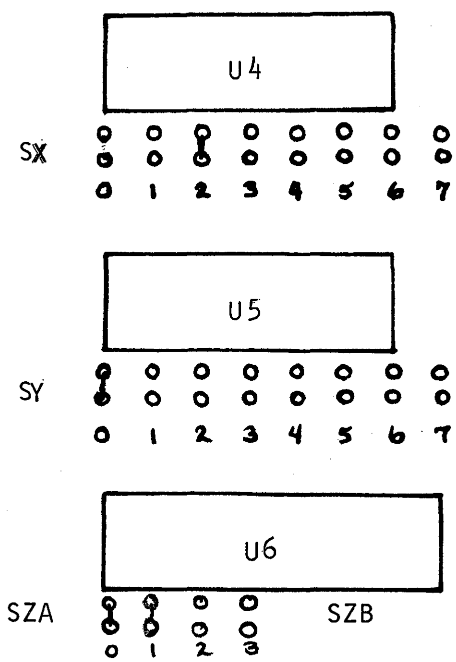
The 7501 uses three cascaded 74LS42 decoders (U4, U5 and U6) to decode address lines A0-A7. These decoders are enabled only when IORQ* and IOEXP* is active. The WR* signal is used to gate the select strobes from U6 that control the output ports.

CHANGING THE 7501 PORT ADDRESS

Refer to the assembly diagram, Document #105195

Locate deocders U4, U5 and U6 (74LS42) adjacent to the STD BUS edge connenctor. Each decoder device has a dual row of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U4 and U5. Make two connections to the matrices adjacent to U6.

The decoder jumper pad numbering figure shows the numbering of the pads adjacent to the decoder chips on the 7501. Also shown are the jumpers (at X2, Y), SZA and SZB) which produce hexadecimal port addresses 40 and 41, the selections made when the card is shipped.



DECODER JUMPER PAD NUMBERING

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

7501 Medium Power DC Output Card Electrical Specifications

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C
R_H	Humidity (1)	5		95	0	95	%RH

User Electrical Characteristics over Recommended Operating Limits

MNEM.	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OL}	Low level user output voltage		.45	0.8	volt
V_{OH}	High level user output voltage			50	volt
I_{OL}	Low level user output current			225	mA
Vc	User-supplied clamp voltage			50	volt
	User output current duty cycle			100	%

STD BUS Electrical Characteristics over Recommended Operating Limits

MNEM.	PARAMETER	MIN.	TYP.	MAX.	UNIT
Icc	STD BUS supply current		600	1000	mA
	STD BUS input load	See STD BUS Edge Connector Pin List			
	STD BUS output drive	See STD BUS Edge Connector Pin List			

Switching Characteristics over Recommended Operating Limits

MNEM.	PARAMETER	FROM	TO	MIN.	TYP.	MAX.	UNIT
T_{PHL}	PROPAGATION TIME	STD DATA BUS	USER IFC		110		nsec.
T_{PLH}	PROPAGATION TIME	"	"		110		nsec.
T_{PHL}	PROPAGATION TIME	USER IFC	STD DATA BUS		110		μsec.
T_{PLH}	PROPAGATION TIME	"	"		110		μsec.

(1) Non-condensing

STD/7501 USER CONNECTOR PIN LIST			
MNEMONIC	PIN NUMBER	PIN NUMBER	MNEMONIC
Ground	2	1	Clamp 0-3
Ground	4	3	Output 0*
Ground	6	5	Output 1*
Ground	8	7	Output 2*
Ground	10	9	Output 3*
Ground	12	11	Clamp 4-7
Ground	14	13	Output 4*
Ground	16	15	Output 5*
Ground	18	17	Output 6*
Ground	20	19	Output 7*
Ground	22	21	Clamp 8-11
Ground	24	23	Output 8*
Ground	26	25	Output 9*
Ground	28	27	Output 10*
Ground	30	29	Output 11*
Ground	32	31	Clamp 12-15
Ground	34	33	Output 12*
Ground	36	35	Output 13*
Ground	38	37	Output 14*
Ground	40	39	Output 15*

User Connector Pin List

STD/7501 EDGE CONNECTOR PIN LIST							
MNEMONIC	INPUT (LSTTL LOADS)	OUTPUT (LSTTL DRIVE)	PIN NUMBER	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*			32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX -V

*Designates Active Low Level Logic

Edge Connector Pin List

SECTION 5

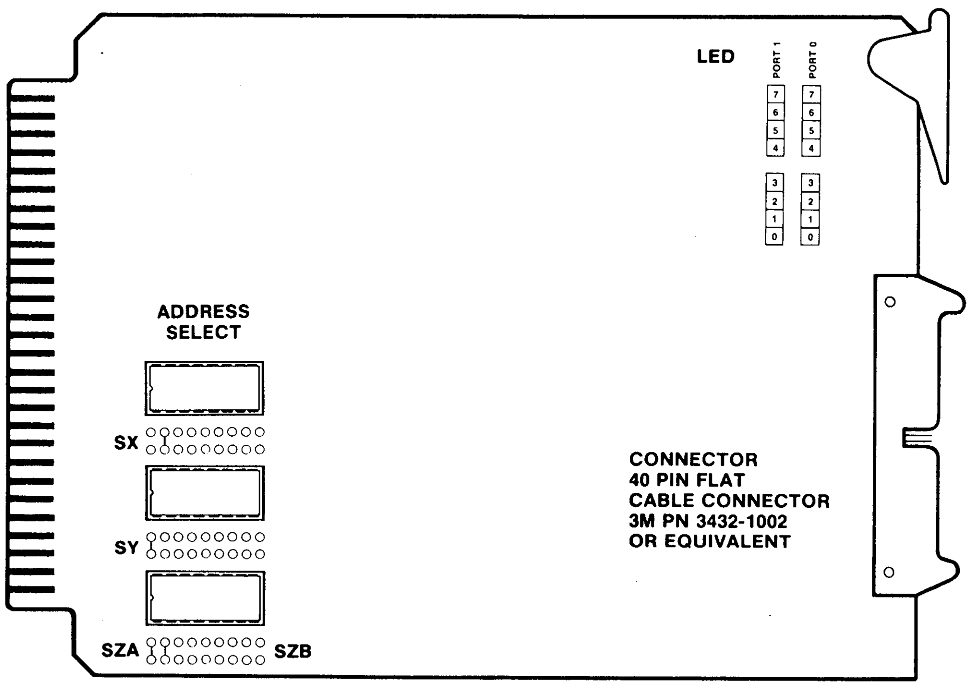
MECHANICAL SPECIFICATIONS

Refer to the Card Address Selection diagram for component placement information.

When placed in a Series 7000 STD BUS card rack, the 7501 requires clearances of 0.150" on the circuit side and 0.600" on the component side of the printed circuit board. These clearances are required for the safety shields on the component side and the circuit side of the 7501.

User Mating Connector Information

The 7501 uses a 40-pin male PC board header connector (3M PN 3432-130 or equivalent). The matching female socket for use in standard flat cable applications is 3M PN 3417-6040.



Card Address Selection

SECTION 6

7501 OPERATING SUBROUTINE MODULES

This section provides flow diagrams and subroutines to operate your 7501 card. These may be used intact, or used as models to construct subroutines for a specific application.

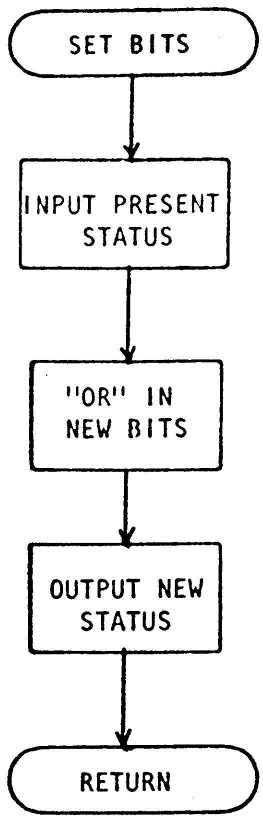
The subroutines are written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7501 port addresses used are the address jumper selections made when the 7501 is shipped.

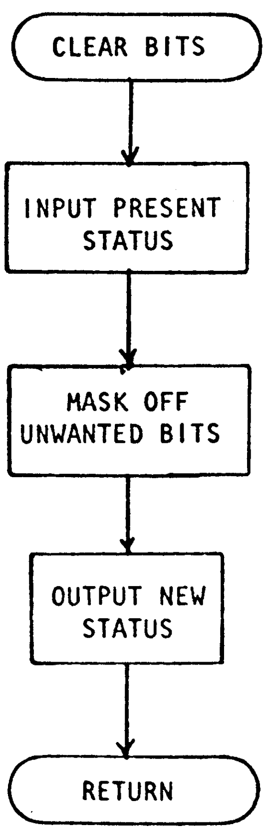
To use these subroutines in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility. The I/O routines provided must be duplicated for the two ports on the 7501. The correct port address must be inserted in each routine.

The flow diagrams presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7501 operation without reference to a particular microprocessor.

The (Set Bit) routine can set a bit or bits on an output port. To use the routine, load the accumulator with the bits that should be changed and set the HL pointer to a place in memory where the port status is stored. Setting a bit will cause the corresponding output driver to sink (conduct) current.

The (Clear Bit) routine can clear a bit or bits on an output port. To use the routine, load the accumulator with the bits that should be changed and set the HL pointer to a place in memory where the port status is stored. Clearing a bit will cause the corresponding output dirver to turn-off (not conduct current).


SET BITS
INPUT PRESENT STATUS
"OR" IN NEW BITS
OUTPUT NEW STATUS
RETURN

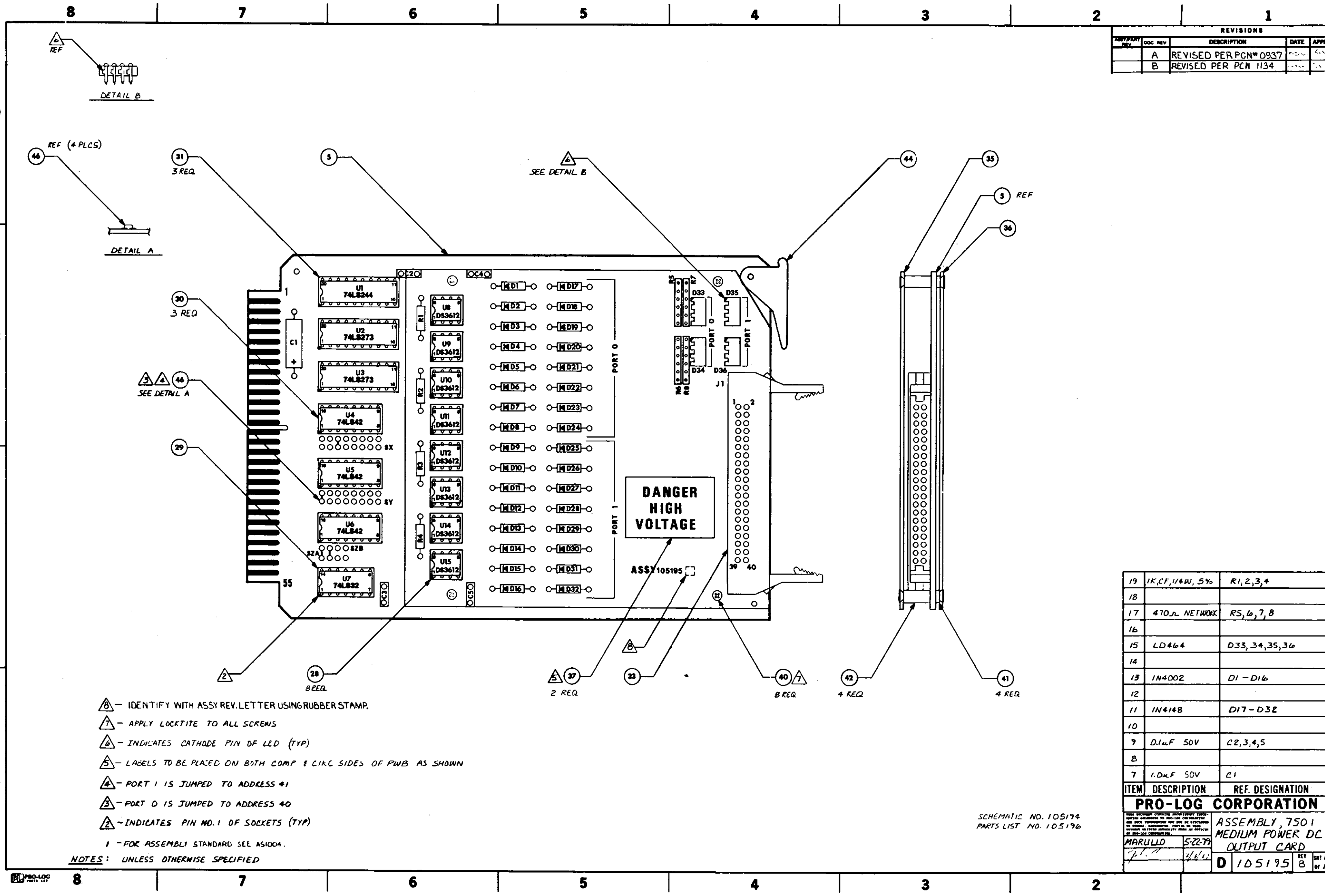

CLEAR BITS
INPUT PRESENT STATUS
MASK OFF UNWANTED BITS
OUTPUT NEW STATUS
RETURN

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

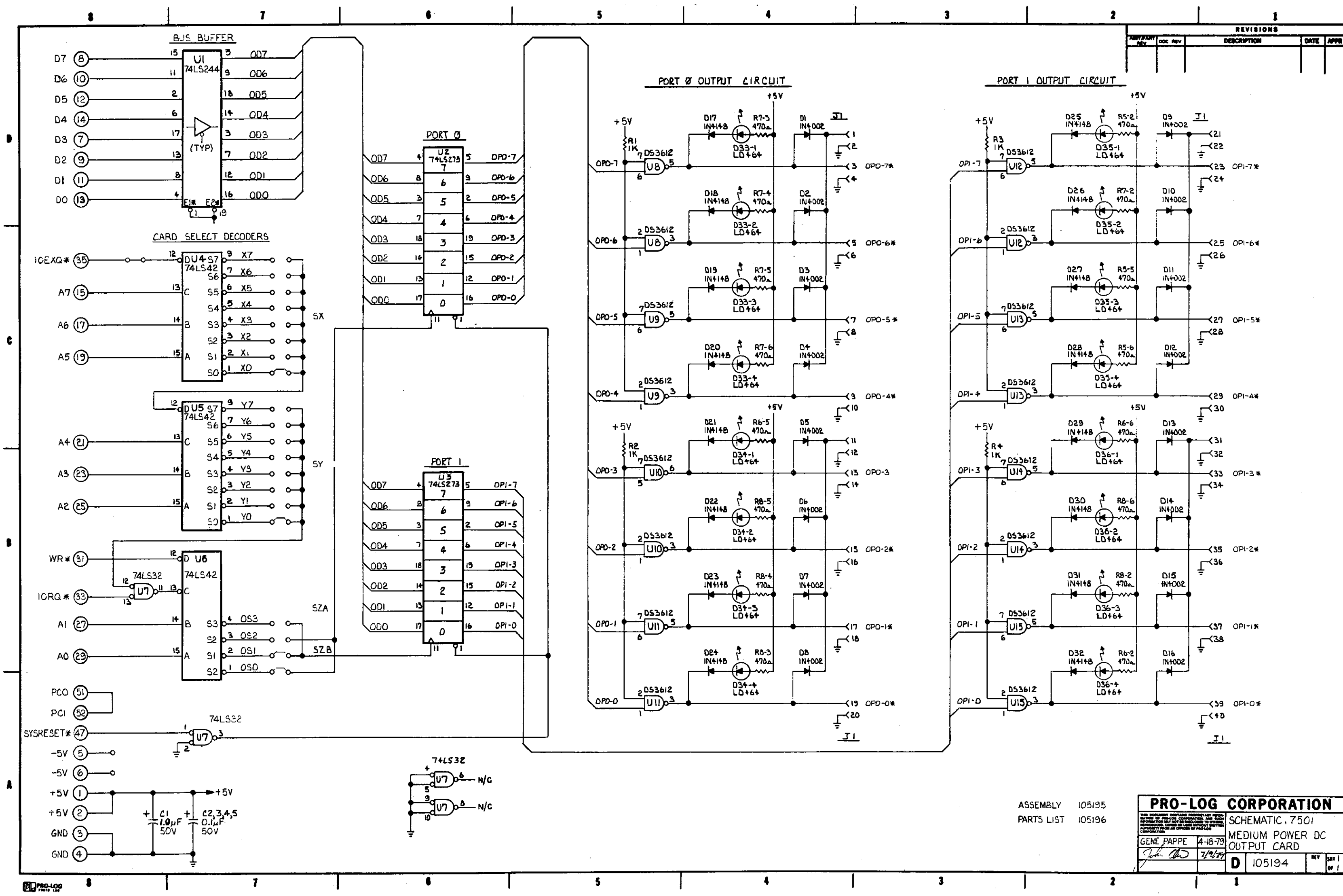
TITLE 7501 DATE

HEXADECIMAL PAGE ADR	LINE ADR	INSTR.	MNEMONIC LABEL	INSTR.	MODIFIER	COMMENTS
	0			LDAI		LOAD A WITH BIT(S) TO BE SET
	1			–	XX	
	2			LDPI	HL	SET MEMORY POINTER
	3			-	XX	
	4			-	XX	
	5	47	(SET BITS)	LDB	A	← SAVE BITS IN B
	6	7E		LDA	M(HL)	← GET PRESENT PORT STATUS
	7	B0		ORA	B	← OR IN NEW BITS
	8	77		STAN	(HL)	← STORE NEW PORT STATUS
	9	D3		OPA		← SEND NEW DATA TO PORT
	A	XX		–	XX	
	B	C9		RTS		
	C					
	D					
	E					
	F					
	0			LDAI		LOAD A WITH BIT(S) TO BE CLEARED
	1			–	XX	
	2			LDPI		SET MEMORY POINTER
	3			-	XX	
	4			-	XX	
	5	2F	(CLEAR BITS)	CMA		COMPLEMENT BITS AND PUT IN B
	6	47		LDB	A	
	7	7E		LDA	M(HL)	← GET PRESENT PORT STATUS
	8	A0		ANA	B	← MASK OF BITS
	9	77		STAN	(HL)	← STORE NEW PORT STATUS
	A	D3		OPA		SEND NEW DATA TO PORT
	B	XX		–	XX	
	C	C9		RTS		
	D					
	E					
	F					

100001 2/77



ITEM	DESCRIPTION	REF. DESIGNATION
19	1K,CF,1/4W, 5%	R1,2,3,4
18		
17	470Ω NETWORK	R5,6,7,8
16		
15	LD464	D33,34,35,36
14		
13	1N4002	D1 – D16
12		
11	1N4148	D17 – D32
10		
9	0.1uF 50V	C2,3,4,5
8		
7	1.0uF 50V	C1


BUS BUFFER
CARD SELECT DECODERS
PORT 0
PORT 1
PORT 0 OUTPUT CIRCUIT
PORT 1 OUTPUT CIRCUIT
REVISIONS
ASSEMBLY 105195
PARTS LIST 105196
PRO-LOG CORPORATION
SCHEMATIC, 7501
MEDIUM POWER DC
OUTPUT CARD
GENE PAPPE 4-18-79
D 105194

USER'S MANUAL

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